Appl. No. 09/607,815
Amdt. Dated February 1, 2006
Reply to Office Action of November 1, 2005

## REMARKS/ARGUMENTS

The Applicant acknowledges the receipt of the Office Action mailed November 1, 2005. Claims 1-4, 7-11, 14–15, 17, 23-24 and 26-33, are currently pending. All of the independent claims, 1-3, 8, 9-10, and 15, have been amended. Reconsideration and allowance of claims 1-4, 7-11, 14–15, 17, 23-24 and 26-33, in their current state, is respectfully requested. The elements of new claim 33 do not contain new matter as the subject matter is described on page 12, lines 10-20 of the original specification.

## I.     Claim Objections

The examiner objected to claims 2, 8, 9 and 23 due to informalities. Accordingly, these claims have been amended to overcome these informalities.

## II.     Claims rejections under 35 U.S.C. 102

Claims 1-4, 6-11, 13-15, 17, 18, 23, 24 and 26-32 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication 2003/0093656 to Masse et al. (*herinafter* Masse). For reasons that will now be set forth, these claims, as currently amended, are not anticipated by Masse.

Independent claims 1-3, 8-10 and 15 as currently amended recite that the count value in the register is adjusted (or incremented/decremented) when the single instruction is executed. By contrast, Masse is for a pipelining system wherein various instructions are stored in the pipeline in various states (see e.g. Figs 5, 6 and 11). Referring to Figure 11 of Masse, an annotated copy of which the applicant has attached to this response, there is shown an instruction flow for a repeat instruction, which is explained in paragraphs 0094-0097. The loop counter in Masse "is tested, decremented and updated during the address stage P3 of the pipeline" (0096). "When the single repeat instruction has terminated, i.e. loop counter 922 value=0 at 1110, the rest of the repeat block is executed" (*Id.*). Because of this, Masse has a latency of four instruction cycles (0094).

-Page 10 of 12-

Appl. No. 09/607,815
Amdt. Dated February 1, 2006
Reply to Office Action of November 1, 2005

In other words, the counter is being decremented before the single instruction to be executed has started executing. Referring to annotated Figure 11 attached hereto, during the third clock cycle (T3) the counter begins to decrement. When the instruction finally begins to execute at the sixth clock cycle (T6), the counter has already reached 0 (see ¶ 0096). Whereas, as now claimed by claims independent claims 1-3, 8-10 and 15 the counter is not decremented until the instruction is being executed, and is decremented (or adjusted) each time the instruction executes.

In addition to the aforementioned reasons, new claim 33 recites that the method is performed in a pre-emptive multi-tasking environment and the single instruction is suspended while a second context executes, and that the contents of an instruction buffer holding the single instruction are preserved while the second process executes. Masse does not teach this. Furthermore, Masse being a pipelined architecture would be subject to the problems discussed in the original specification (i.e. the loop can become un-cached when the next context executes since the locality of reference is lost; therefore when the suspended loop is resumed loop performance may suffer). An aspect of claim 33 is that because the instruction buffer is preserved the instruction can begin executing at the point where the suspension occurred with no further overhead (whereas Masse would have another 4 cycle latency period before executing).

### III.    Conclusion

For the reasons just set forth Independent claims 1-3, 8-10, and 15 as currently amended are not anticipated by the cited prior art. Claims 4, 7, 11, 14, 17, 23-24 and 26 -33 are directly dependent from one of claims 1-3, 8-10, and 15 and for the same reasons are not anticipated by the cited prior art.

If the Examiner believes there are any further matters that need to be discussed in order to expedite the prosecution of the present application, the Examiner is invited to contact the undersigned. If there are any other fees necessitated by the foregoing communication, please
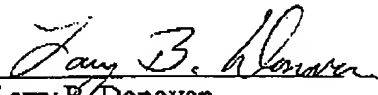
Appl. No. 09/607,815
Amdt. Dated February 1, 2006
Reply to Office Action of November 1, 2005

charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. (72255/02662).

Respectfully submitted,

TUCKER ELLIS & WEST LLP

Date: February 1, 2006

Larry B. Donovan
Registration No. 47,230
1150 Huntington Building
925 Euclid Avenue
Cleveland, Ohio 44115-1475
Customer No. 23380
(216) 696-3864 (phone)
(216) 592-5009 (fax)

-Page 12 of 12-

72255/02662/870808/1